Dry etching of a Silicon Nitride cell

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In this paper we will describe the Self Aligned dry etch definition of a memory cell characterized by an Al_2O_3 high-k dielectric layer and by a Silicon Nitride Floating Gate. We will show our results with a particular focus on the strategy to avoid the lateral erosion of the Poly Silicon Control Gate during the Silicon Nitride etch.

Introduction

The progressive dimension downscaling of electronic devices leads to the investigation of new materials for the dielectric layer and the Floating Gate of the new generation Flash memory cells. In particular, the thinning of the dielectric layer pushes towards the employment of high-k materials. The new materials for the Floating Gates should suffer less dopant depletion and should have higher equivalent capacitive thickness than the traditional Poly Silicon.

The main process challenge during the Self Aligned definition of these structures is the extreme thinness of the various films: the dielectric layer, the Floating Gate and the stopping layer (the tunnel SiO_2) are only a few nm thick. Slow and very selective etch recipes are therefore mandatory to avoid active area damages and to guarantee the robustness of the process.

Experimental

In Fig. 1 we show the film stack that we should define. The cell is formed by a PolySi Control Gate, by a high-k dielectric layer (Al_2O_3) and by a SiN Floating Gate. The Al_2O_3 and the SiN films, as well as the SiO_2 tunnel (our stopping layer) are only a few nm thick.

The mask pattern is reproduced lithographically through a 193 nm PhotoResist, exposed over an antireflective organic layer (BARC). The memory cell has asymmetrical surroundings: the drain line is wider (almost the double) than the source.

The tool employed to process the wafers is a Lam 2300 Versys Star T etcher.

Results and discussion

The definition of the stack does not require any particular solutions until the high-k layer is reached. We etch the BARC with a Cl_2/O_2 plasma, followed by a slow O_2 Trim step to tune the CD. Then we etch the PolySi Control Gate with an HBr/Cl_2 main etch and a slower Overetch. This step lands on the Al_2O_3 surface and removes all the PolySi residuals without damaging the high-k layer. The Al_2O_3, in fact, is very hard to etch and the standard PolySi etch chemistries have no effects on it.

The process challenges begin at this level. Since the dielectric layer, the Floating Gate and the tunnel Oxide are very thin, we have to etch every film very selectively to the underlying one. Besides preserving the active areas, this allows us to set optical Endpoints on the Al_2O_3 and SiN steps and to compensate undesired loading effects caused by the asymmetry of the pitch.

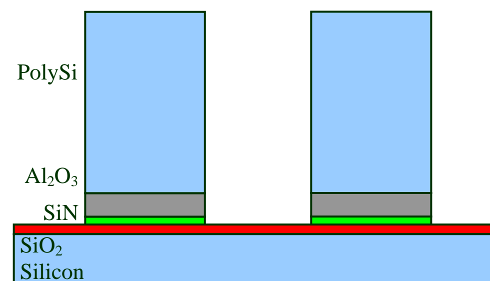

Fig.1: picture of the film stack after complete etch and PhotoResist removal.

To reach high selectivity to SiN we must etch Al_2O_3 slowly. The Al_2O_3 etch rate, however, must be greater than ~20 nm/min to prevent etch stop caused by micro-loading effects. Therefore, we process the Al_2O_3 in two passages: a main etch with higher etch rate but lower selectivity which allows setting an optical Endpoint. Then we perform a slower but very selective Overetch (sel. > 25) removing all the residuals.

To be selective over SiN, the Al_2O_3 etch must be mainly chemical: we use BCl_3 based recipes, reducing the d.c. bias voltage as much as possible not to meet etch stop effects. We also noticed that the selectivity increases with the

wafer temperature: the selectivity over SiN doubles raising the ESC temperature by 20°C. We set in the recipe the highest ESC temperature value allowed by the tool. The best recipes are also very selective towards PolySi: the Control Gate does not suffer for lateral erosion during the Al_2O_3 definition.

This ideal condition can not be reached during the SiN etch: the recipe with higher selectivity over SiO_2 is very aggressive towards the PolySi. In fact, using a mix of CF_4, HBr, O_2 and $SiCl_4$ with no d.c. bias voltage, we etch SiN 40 times faster than SiO_2, but the etch rate over PolySi is much larger than both. This produces an unbearable lateral erosion of the Control Gates (see Fig.2).

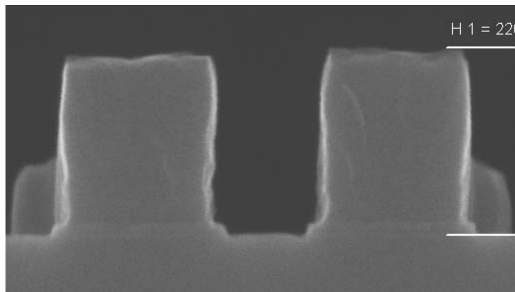

Fig.2: the memory cells defined with the traditional approach. The PolySi Control Gates are strongly damaged by the SiN step chemistry.

Since we can not improve the selectivity of the SiN step over PolySi without losing that over SiO_2, we followed a new etch strategy exploring the possibility to protect the cell sidewalls before defining the Floating Gate.

The excellent selectivity over SiO_2 of our best SiN recipe suggested us the opportunity to oxidize the PolySi Control Gate walls before starting the SiN step. In this way, when the last step of the recipe defines the SiN Floating Gate, a thin layer of SiO_2 is already grown all over the PolySi Control Gate. Any erosion of the cell is prevented by the high selectivity of the SiN recipe over SiO_2.

Therefore we modified the recipe introducing an Oxygen Flash, immediately after the Al_2O_3 Overetch. The Flash must be long enough to guarantee the complete PhotoResist removal (clear optical EndPoint) and the subsequent oxidation of the cell top (long Overetch). In Fig.3 we show the results obtained through this strategy: the sidewalls and the top of the Control Gate are not damaged. The weak Silicon oxidation occurring during the O_2 Flash is enough to shield the PolySi from the aggressive chemistry used to define the SiN Floating Gate.

Conclusions

In this work we present the results about the Self Aligned definition of a memory cell formed by a PolySi Control Gate, by a high-k Al_2O_3 dielectric layer and by a SiN Floating Gate. We developed very slow and selective recipes to etch the very thin dielectric layer and Floating Gate without damaging the tunnel Oxide.

In particular we show an innovative approach to avoid the lateral erosion of the cell through an in situ oxidation. Performing an O_2 Flash before the Floating Gate definition and using in the last step a chemistry very selective over SiO_2, the cell sidewalls are preserved. The O_2 Flash duration must be calibrated to remove the PhotoResist and to oxidize the Control Gate top: the high selectivity over SiO_2 of the Floating Gate step prevents the cell top from being damaged.

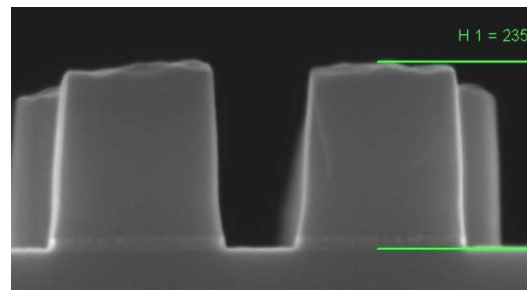

Fig.3: the memory cell defined with the new strategy. The O_2 Flash prevents the erosion of the PolySi Control Gate during the SiN step.