Integration of Wet Clean and Plasma Etch Processing for Enhanced Process Control in Semiconductor Manufacturing

I. Vos[1], D. Hellin[2], J. Vertommen[2] and W. Boullart[1]

[1]*IMEC, Kapeldreef 75, 3001 Leuven, Belgium*
[2]*Lam Research Corporation, Kapeldreef 75, 3001 Leuven, Belgium*
Email: Ingrid.Vos@imec.be

This paper explores the benefits of the integration of wet cleaning using short and controlled exposure times with plasma dry etch processes. Selectivity for the post-etch residues versus substrate loss and the effect of delay time between etch and clean processes are investigated for shallow trench isolation (STI), poly-silicon gate and contact clean applications.

Introduction

The continuous downscaling of transistor dimensions in every new semiconductor technology node sets more aggressive process specifications. In cleaning technology, one strives to continuously reduce the loss of substrate and film thickness while maintaining a high cleaning efficiency.

The novel concept of Confined Chemical Cleaning™, developed by Lam Research Corporation, anticipates on these requirements by enabling short and well-controlled exposure times using more concentrated chemical solutions. In addition, reducing delay time between etching and subsequent wet clean by introducing clustered processing may allow for more effective residue removal.

Experimental

This study utilizes a Lam Research 2300® platform integrating a prototype wet clean module with conductor etch, dielectric etch and dry strip modules. With the Confined Chemical Cleaning™ technology, a cleaning head scans the wafer surface with a high flow fluid stream, ensuring continuous chemical replenishment and fast by-product removal. Exposure times for the cleaning process are in the order of 2 seconds.

Results and discussion

Shallow trench isolation. After etch and dry strip, residues of variable thickness were present on the sidewall of the structure, as is observed in TEM and SEM (Fig. 1a and 1c). The residues were cleanable immediately after etch using 1% HF at 65 °C with an exposure time of 2 seconds (Fig. 1b and 1d). No lateral attack of the pad oxide was observed. However, the ability to remove these residues using the same cleaning process diminished with increasing delay between etch and wet clean. A delay time of 1 hour, comparable to normal queue times in semiconductor manufacturing, had a significant impact on the cleaning performance. This effect was observed for delay times as short as 15 minutes (Fig. 1e and 1f).

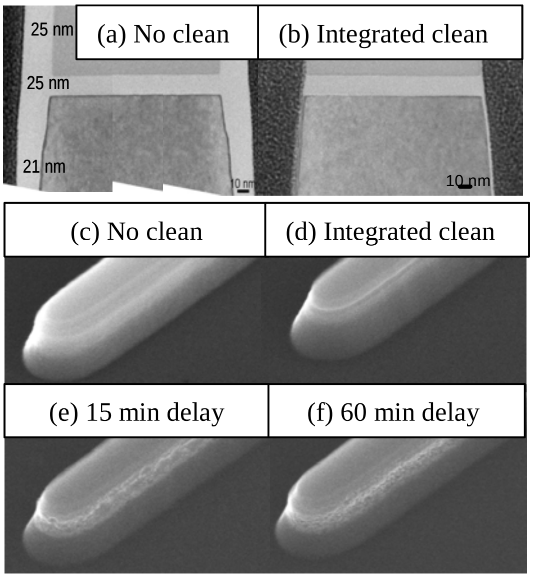
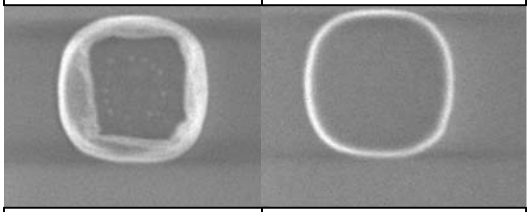


Figure 1: Evaluation of residue removal and substrate loss for post-etch residues on an STI structure using a cleaning process of 1% HF at 2 seconds exposure time.

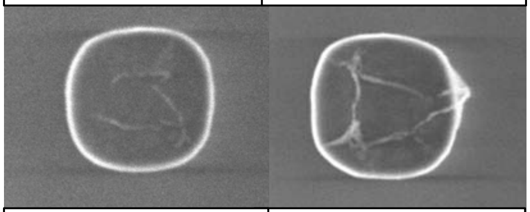
Poly-silicon gate. In order to produce visible residues, the hardmask-based poly-silicon etch process was detuned by omission of the photo-resist strip between the hardmask and poly-silicon etch steps (Fig. 2a). Clean structures were obtained after integrated etch, dry strip and wet clean using 1% HF at 68°C with a

2-second cleaning exposure (Fig. 2b). Delayed cleans resulted in reduced cleaning performance, and the effect becomes more pronounced for longer delay times (Fig. 2c and 2d). The effect of the wet clean chemistry on cleaning of aged residues was investigated using dilute HF solutions. Results showed that for the same cumulative exposure (time × concentration), a short clean with a more concentrated solution was superior to a longer clean with a more dilute solution (Fig. 2e and 2f).

(a) No clean | (b) Integrated clean



(c) 1 hour delay | (d) 24 hours delay



(e) 1% HF, 2 sec | (f) 0.17% HF, 12 sec

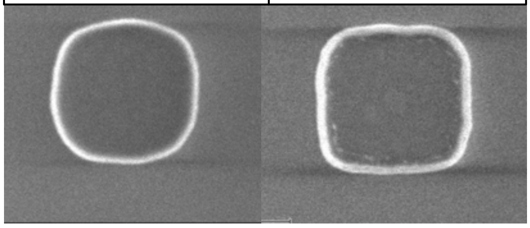
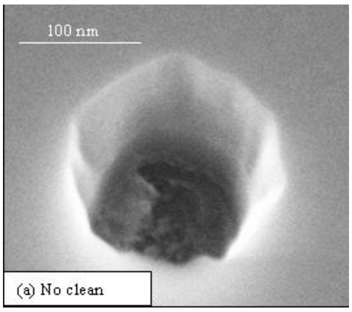
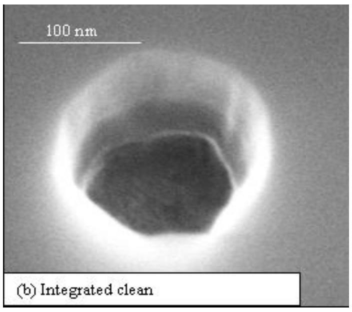


Figure 2: Evaluation of delay time (a-d) and chemical exposure (concentration x time) on aged residue removal after a hardmask based poly-silicon etch (e and f).

Contact etch. After contact etch in a 65 nm node short loop process flow, XPS revealed the presence of C, F and O containing species on the bottom and the sidewalls of the contact holes. The residues were cleanable using an ammonia/peroxide solution (APM) at 65 °C (Fig. 3a and 3b). The substrate loss, as evaluated on blanket wafers, was below the spectroscopic ellipsometer detection limits. The process flow was completed with contact metallization and a Cu/low-k based single damascene module for electrical evaluation. Wafers with integrated clean (effectively no delay time) showed the highest yield and good within-wafer non-uniformity for the Kelvin resistance. A distinct resistance increase and yield loss (more than 30% loss) is observed with increasing delay time (Fig. 3c), indicating that control of the delay time between etch/dry strip and wet clean is critical. Integrating etching and cleaning processes is an effective method to obtain high yielding and uniform contact resistance distribution over the wafer.





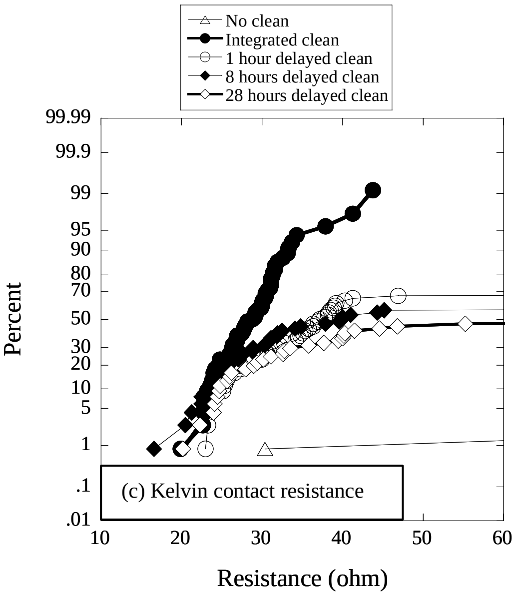


Figure 3: Evaluation of post-etch residue removal in 90 nm contacts with an APM clean. Delayed clean deteriorates Kelvin contact resistance values and leads to yield loss.

Conclusions

It was demonstrated that the Confined Chemical Cleaning™ technology enables highly selective cleaning of post-etch residues without significant substrate loss or undercut. Moreover, integrating etch and clean processes results in a higher performance and robustness of the cleaning process.